REMARKS

Claims 1, 4-6 and 9-21 are pending in the application.

Claims 1, 4-6 and 9-21 have been rejected.

Claims 1 and 11 have been amended, as set forth herein.

Claims 17 and 18 have been canceled, without prejudice.

I. REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 4-6, and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiussi (U.S. Published Patent Application No. 2003/0142624) in view of Moore (U.S. Published Patent Application No. 2004/0136370).

Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiussi in view of Moore and further in view of Hill (U.S. Published Patent Application No. 2003/0035422).

Claims 11-13, 16-18, and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Karawai (U.S. Published Patent Application No. 2001/0033581) in view of Chiussi and Moore.

Claims 14, 15, 19, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Karawai, Chiussi, and Moore and further in view of Dell (U.S. Published Patent Application No. 2002/0085578).

The rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does

not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142. In making a rejection, the examiner is expected to make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), *viz.*, (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the art. In addition to these factual determinations, the examiner must also provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (*In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir 2006) (cited with approval in *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007)).

As described in the Applicant's specification (published PCT application), Applicant's demultiplexer separates the input data into GT (guaranteed throughput) and BE (best effort) data which fill their respective input buffers (GT input buffers 2 and BE input buffers 3). A combined control means (6, 6-1, 6-2) controls multiplexers which selectively pass individual data streams (GT or BE) to the data switch (5). At least one GT input buffer (2) is selectively coupled to at least one data switch input by the combined control means, in a contention fee manner (see the third GT buffer in Figure 1(a)). See, Applicant's specification, Figure 1(a), pp. 4-5.

Claim 1 has been amended to recite "at least one guaranteed throughput input buffer selectively coupled to at least one data switch input by the combined control means."[1]

This is in contrast to the disclosure of Chiussi, wherein a receiver 600 uses the contents of a flow identification field contained in the header of each incoming packet to identify the data packet flow of the packet. The identified flow can be either a guaranteed bandwidth (GB) or a best effort flow. Chiussi, para. 0049. The GB flow queue (which the Examiner states is equivalent to the guaranteed throughput input buffer of the present invention) is stored in packet RAM 607 which is permanently coupled to the data switch input via the packet transmitter 601. Chiussi, para. 0048. There is no pre-separation into separate incoming data streams with a combined control. Therefore, Chiussi does not disclose a GT input buffer which is selectively coupled to at least one data switch input by the combined control means. The GB flow queue in Chiussi is permanently coupled to the switch. This advantageous feature of the claimed invention saves both hardware and software scheduling control requirements. Chiussi does not disclose, teach or suggest this feature.

Further, independent Claim 1 has been amended to distinguish between the inputs of the data switching device (at the extreme left in Fig. 1(a) and the inputs (I1-I4)/outputs O1-O4) of the data switch. Claim 1 now includes "an incoming stream of guaranteed throughput data" and "an incoming stream of best effort data" and "data switch inputs for guaranteed throughput and best effort data."[2]

In addition, independent Claim 1 (and independent Claim 11) has been amended to include the features of original dependent claims 17 and 18 to recite that the device comprises "guaranteed throughput control means to schedule the guaranteed throughput data in one step, wherein the one step comprises at least a one of a reservation of at least one data switch input of the switching matrix and a reservation of at least one data switch output."

As described in the specification and Fig. 2(a), the GT control means 6-1 reserves a GT

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[1] Support for this amendment can be found in Fig. 1(a), Fig. 2(a) and page 4, lines 14-15.

[2] Support for this amendment can be found in Fig. 1(a) and original dependent claim 20.

connection between one of the inputs (I1-I4) and one of the outputs (O1-O4) -- indicated by an encircled 1 in Fig. 1(a). Any BE request from the reserved GT connection input to any output of the data switch is disabled, therefore no BE data is sent to the same data switch input as the GT data (as shown in Fig. 2(d)). This simplifies the BE scheduling because a smaller amount of inputs have to be taken into account during the BE request phase (see, Fig. 2(b)).

In distinct contrast, the WRR scheduler in Chiussi modifies the operation of a basic WRR scheduler by dividing the service frame 406 into two subframes. In the first subframe 407, the primary WRR scheduler (PWS) 401 fulfills the bandwidth requirements of the GB flows 402. In the second subframe 408, the PWS 401 distributes fair service to the plurality of BE flows 405. The service frame containing both GB and BE flows are sent on the same "outgoing link" to an input of the data switch.

As such, Applicant asserts that Chiussi fails to disclose, teach or suggest one or more of the elements/features (as described above) recited in amended independent Claim 1.

Similarly, Applicant submits that Moore does not disclose a data switching device comprising, with respect to independent Claim 1, an incoming stream of best effort data, combined control means for controlling data scheduling of the incoming streams such that the best effort data scheduling is based on contention free guaranteed throughput scheduling, or at least one guaranteed throughput input buffer selectively coupled to at least one data switch input by the combined control means.

Therefore, the proposed combination of Chiussi with Moore fails to disclose, teach or suggest each and every element/feature recited in independent Claim 1 (and its dependent Claims).[3]

With respect to the rejection(s) of independent Claim 11, this claim has been amended to include "best effort control means to selectively fill said best effort input buffers with best effort data and schedule the best effort data."[4] Similar to independent Claim 1, this Claim 11 has has also been

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[3] Similarly, it does not appear that Hill cures the deficiencies noted in Chiussi and Moore, and therefore, dependent Claim 10 is believed patentable over the proposed combination.

[4] Support for this amendment can be found on page 5, lines 5-6 and Fig. 1(a).

amended to include the features of original dependent claims 17 and 18 to recite that the device comprises "guaranteed throughput control means to schedule the guaranteed throughput data in one step, wherein the one step comprises a one of at least a reservation of at least one data switch input of the switching matrix and a reservation of at least one data switch output.

In Claim 11, the combined scheduling control means operates such that the GT control means first reserves a connection between one of the inputs (I1-I4) and one of the outputs (O1-O4) of the data switch. The BE control means then selectively fills the BE input buffers with best effort data as indicated by the crossed BE input buffers 3 in Fig. 1(a).

This is in contrast to the disclosure of Chiussi wherein if the identified packet flow is a best effort flow, the best effort flow is automatically stored in the BE flow queue 505 (which the Examiner states is equivalent to the best effort input buffer of the present invention). Chiussi does not disclose the advantageous feature of a plurality of best effort input buffers coupled as inputs to the plurality of multiplexers wherein the combined scheduling control means includes a best effort control means to selectively fill the best effort input buffers with best effort data to simplify the best effort scheduling. Thus, Applicant asserts that amended Claim 11 is not disclosed, taught or suggested by Chiussi.

Similarly, Applicant respectfully submits that Moore does not disclose a data switching device comprising, with respect to independent Claim 11, a plurality of multiplexers coupled to the plurality of inputs of a switching matrix, a plurality of best effort input buffers coupled as inputs to the plurality of multiplexers, a guaranteed throughput input buffer coupled as another input to a first multiplexer of the plurality of multiplexers, or a combined scheduling control means coupled to the plurality of multiplexers comprising guaranteed throughput control means and best effort control means.

Therefore, the proposed combination of Chiussi with Moore fails to disclose, teach or suggest each and every element/feature recited in independent Claim 11 (and its dependent Claims).[5]

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[5] Similarly, it does not appear that Dell cures the deficiencies noted in Chiussi and Moore, and therefore, dependent Claims 14-15 and 19-20 are believed patentable over the proposed combination.

In sum, Applicant submits at least the following as reasons the claims are patentable over the cited art of record:

1) Neither Chiussi nor Moore disclose the element(s)/feature(s) of amended Claim 1 that "at least one guaranteed throughput input buffer selectively coupled to at least one data switch input by the combined control means;

2) Neither Chiussi, Moore, or Karawi disclose the element(s)/feature(s) of amended Claim 11 of "best effort control means to selectively fill said best effort input buffers with best effort data and schedule the best effort data for transfer through the switching matrix to another one of the plurality of outputs of the switching matrix, wherein best effort control means is further configured to schedule the best effort data based on a contention free guaranteed throughput scheduling"; and

3) Neither Chiussi nor Moore discloses, with respect to independent Claims 1 and 11, reserving a GT connection input to any output of the data switch so that no BE data is sent to the same data switch input as the GT data to simplify the BE scheduling.

Accordingly, the Applicant respectfully requests withdrawal of the § 103(a) rejection of Claims 1, 4-6, 9-16 and 19-21.

II. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***rmccutcheon@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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